EN CONTROLL OF PRINCES

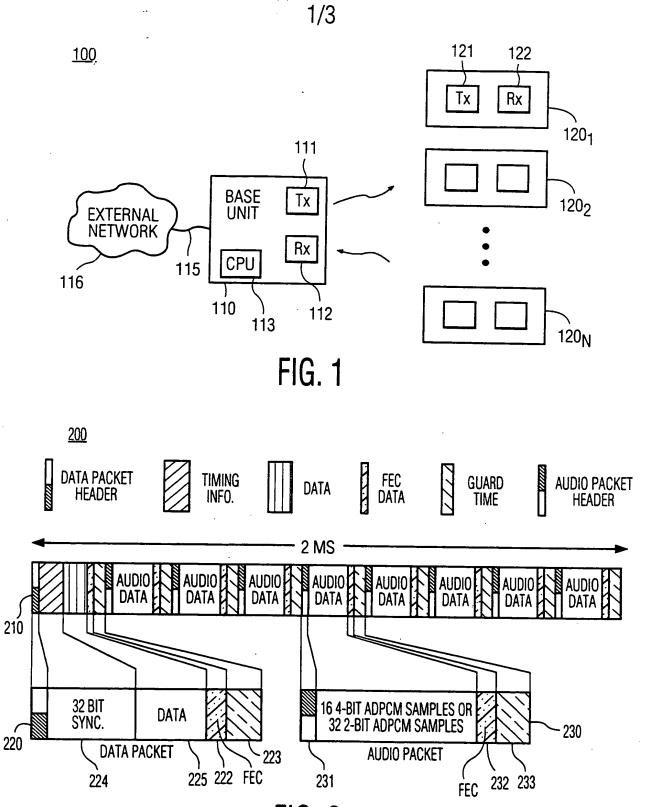


FIG. 2

outs much 2000

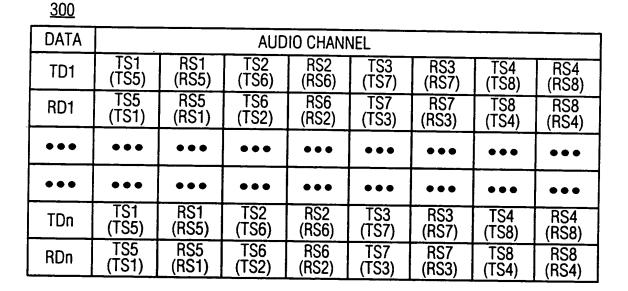


FIG. 3

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DATA		AUDIO CHANNEL							
TD1	T1 (T5)	R1 (R5)	T2 (T6)	R2 (R6)	T3 (T7)	R3 (R7)	T4 (T8)	R4 (R8)	
RD1	T5 (T1)	R5 (R1)	T6 (T2)	R6 (R2)	T7 (T3)	R7 (R3)	T8 (T4)	R8 (R4)	
TD2	T1	R1	T2	R2	T3	R3	T4	R4	
	(T5)	(R5)	(T6)	(R6)	(T7)	(R7)	(T8)	(R8)	
RD2	T5	R5	T6	R6	T7	R7	T8	R8	
	(T1)	(R1)	(T2)	(R2)	(T3)	(R3)	(T4)	(R4)	
TD3	T1	R1	T2	R2	T3	R3	T4	R4	
	(T5)	(R5)	(T6)	(R6)	(T7)	(R7)	(T8)	(R8)	
RD3	T5	R5	T6	R6	T7	R7	T8	R8	
	(T1)	(R1)	(T2)	(R2)	(T3)	(R3)	(T4)	(R4)	
TD4	T1	R1	T2	R2	T3	R3	T4	R4	
	(T5)	(R5)	(T6)	(R6)	(T7)	(R7)	(T8)	(R8)	
RD4	T5	R5	T6	R6	T7	R7	T8	R8	
	(T1)	(R1)	(T2)	(R2)	(T3)	(R3)	(T4)	(R4)	
TD5	T1	R1	T2	R2	T3	R3	T4	R4	
	(T5)	(R5)	(T6)	(R6)	(T7)	(R7)	(T8)	(R8)	
RD5	T5	R5	T6	R6	T7	R7	T8	R8	
	(T1)	(R1)	(T2)	(R2)	(T3)	(R3)	(T4)	(R4)	
TD6	T1	R1	T2	R2	T3	R3	T4	R4	
	(T5)	(R5)	(T6)	(R6)	(T7)	(R7)	(T8)	(R8)	
RD6	T5	R5	T6	R6	T7	R7	T8	R8	
	(T1)	(R1)	(T2)	(R2)	(T3)	(R3)	(T4)	(R4)	
TD7	T1	R1	T2	R2	T3	R3	T4	R4	
	(T5)	(R5)	(T6)	(R6)	(T7)	(R7)	(T8)	(R8)	
RD7	T5	R5	T6	R6	T7	R7	T8	R8	
	(T1)	(R1)	(T2)	(R2)	(T3)	(R3)	(T4)	(R4)	
TD8	T1	R1	T2	R2	T3	R3	T4	R4	
	(T5)	(R5)	(T6)	(R6)	(T7)	(R7)	(T8)	(R8)	
RD8	T5	R5	T6	R6	T7	R7	T8	R8	
	(T1)	(R1)	(T2)	(R2)	(T3)	(R3)	(T4)	(R4)	

FIG. 4